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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/712,364	11/12/2003	Kazuo Kobayashi	51508/DBP/A400	1459
23363	7590	01/05/2006	EXAMINER	
CHRISTIE, PARKER & HALE, LLP PO BOX 7068 PASADENA, CA 91109-7068				COLEMAN, WILLIAM D
ART UNIT		PAPER NUMBER		
2823				

DATE MAILED: 01/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/712,364	KOBAYASHI, KAZUO
	Examiner	Art Unit
	W. David Coleman	2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 17 October 2005.

2a) This action is FINAL. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 16-21 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 16-21 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:

1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)

2) Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.

4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.

5) Notice of Informal Patent Application (PTO-152)

6) Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on October 17, 2005 has been entered.

Claim Rejections - 35 USC § 102

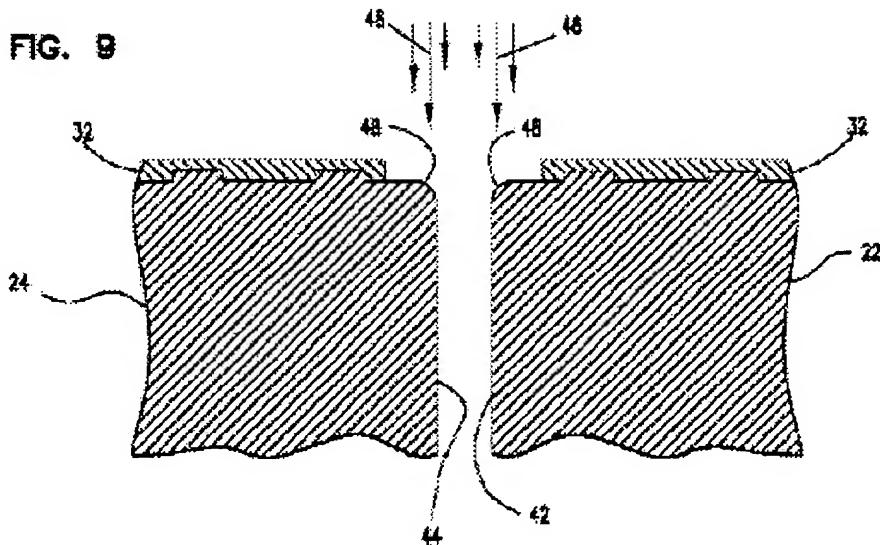
2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 16, 17, 19, 20 and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Jones, U.S. Patent Application Publication No US 2001/0034564 A1. Jones discloses a semiconductor wafer machining method as claimed. See FIGS. 1-14, where Jones teaches the following limitations.

FIG. 9



4. Pertaining to claim 16, Jones teaches a semiconductor wafer machining method for machining a semiconductor wafer, comprising the steps of: carrying out an entire cut through the semiconductor wafer with a cutting blade to form lateral surfaces (the Examiner takes the position that it is well known to dice a integrated circuit having a backing tape with a wheel saw); and Jones teaches irradiating the lateral surfaces of the cut with laser light to form a modified layer by melting (because Jones teaches that this technique is used for IC's see paragraph [0020], all the limitations of the claim are met).

5. Pertaining to claim 17, Jones teaches the semiconductor wafer machining method according to claim 16, wherein an entirety of the lateral surfaces of the semiconductor wafer is irradiated with the laser light (see first and second embodiment).

6. Pertaining to claim 19, Jones teaches the semiconductor wafer machining method according to claim 16, wherein a dicing tape is adhered to a surface of the semiconductor wafer; and

the laser light is irradiated after cutting only the semiconductor wafer and expanding the dicing tape (the Examiner takes the position that the laser will expand and melt the backing tape prior to the melting of the IC since the melting temperature of the adhesive backing tape is much lower than a semiconductor IC).

7. Pertaining to claim 20, Jones teaches the semiconductor wafer machining method according to claim 16, wherein the laser light is irradiated onto the lateral surface of a first cut that has been already formed and is different from a second cut being formed by the cutting blade (see FIGS. 3 and 4).

8. Pertaining to claim 21, Jones teaches the semiconductor wafer machining method according to claim 16, wherein the laser light is irradiated onto the lateral surfaces of the cut that is being formed by cutting the semiconductor wafer by the cutting blade while following the movement of the cutting blade (the Examiner has provided several references which teach the conventional method of cutting the semiconductor wafer by the cutting blade while following the movement of the cutting blade).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

Art Unit: 2823

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

10. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jones U.S. Patent Application Publication No. US 2001/0034564 A1 in view of Manor U.S. Patent Application Publication No. US 2002/0031899 A1.

11. Jones fails to specifically teach the semiconductor wafer machining method according to claim 16, wherein the laser is a YAG laser or a CO2 laser. Manor teaches wherein dicing a wafer incorporates a CO2 laser. In view of Manor, it would have been obvious to one of ordinary skill to incorporate the features of Manor into the Jones semiconductor process because it provides a method for singulating semiconductor wafers (see Abstract).

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to W. David Coleman whose telephone number is 571-272-1856. The examiner can normally be reached on Monday-Friday 9:00 AM - 5:30 PM.

13. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

14. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



W. David Coleman
Primary Examiner
Art Unit 2823

WDC